WHAT IS CLAIMED IS:

1. A voltage regulator comprising:

a first stage capable of receiving a reference voltage and capable of having a first current flowing through the first stage;

a second stage, coupled to the first stage, capable of having a second current flowing through the second stage; and

a third stage, coupled to the second stage, capable of outputting an output voltage and capable of having a third current flowing through the third stage,

wherein the first, second and third currents are proportional to each other throughout a range of operation of the voltage regulator between substantially zero output current and maximum output current.

2. The regulator of claim **1**, wherein the third stage includes a pass transistor, and the second stage includes a first mirror transistor and an input transistor in series with the first mirror transistor, and

wherein a gate of the first mirror transistor is driven by the same voltage as a gate of the pass transistor.

3. The regulator of claim **2**, wherein the first stage includes a second mirror transistor, wherein a gate of the second mirror transistor is driven the same voltage as the gate of the pass transistor.

4. The regulator of claim **3**, further including a low pass filter between the gate of the second mirror transistor and the gate of the first mirror transistor.

5. The regulator of claim **4**, wherein the low pass filter is an RC network.

6. The regulator of claim **4**, wherein the first stage includes a first trickle current source in parallel with a current source that is parallel with the first mirror transistor.

7. The regulator of claim **6**, further including a second trickle current source supplying a trickle current to the second stage.

8. The regulator of claim **6**, further including a first shut off transistor in series with the first mirror transistor and the input transistor of the second stage, a gate of the shut off transistor being driven by an opamp,

wherein the opamp inputs the reference voltage at a first input, and voltage from a resistor divider at a second input.

9. The regulator of claim **8**, further including a second shut off transistor in series with the second mirror transistor and the input transistor of the first stage, a gate of the second shut off transistor being driven by an opamp.

10. The regulator of claim **8**, further including a current source between the resistor divider and the supply voltage.

11. The regulator of claim **8**, further including an NMOS transistor between the first shut off transistor and the input transistor.

12. The regulator of claim **1**, wherein a phase margin of the voltage regulator is at least 60 degrees.

13. The regulator of claim **1**, further including a feedback stage with a resistor divider between the third stage and the first stage, wherein a feedback voltage from the resistor divider controls an amplification of the first stage.

14. The regulator of claim **1**, wherein a drop-out voltage of the regulator is no more than approximately 14 millivolts.

15. A voltage regulator comprising:

a first stage receiving a reference voltage and having a first current flowing through the first stage;

a second stage having a second current flowing through the second stage; and

a third stage outputting an output voltage and having a third current flowing through the third stage,

wherein the first stage drives the second stage as a low input impedance load.

16. The regulator of claim **15**, wherein the third stage includes a pass transistor, and the second stage includes a first mirror transistor and an input transistor in series with the first mirror transistor, and

wherein a gate of the first mirror transistor is driven by the same voltage as a gate of the pass transistor.

17. The regulator of claim **16**, wherein the first stage includes a second mirror transistor, wherein a gate of the second mirror transistor is driven the same voltage as the gate of the pass transistor.

18. The regulator of claim **17**, further including a low pass filter between the gate of the second mirror transistor and the gate of the first mirror transistor.

19. The regulator of claim **18**, wherein the low pass filter is an RC network.

20. The regulator of claim **18**, wherein the first stage includes a first trickle current source in parallel with a current source that is parallel with the first mirror transistor.

21. The regulator of claim **20**, further including a second trickle current source supplying a trickle current to the second stage.

22. The regulator of claim **20**, further including a first shut off transistor in series with the first mirror transistor and the input transistor of the second stage, a gate of the shut off transistor being driven by an opamp,

wherein the opamp inputs the reference voltage at a first input, and voltage from a resistor divider at a second input.

23. The regulator of claim **22**, further including a second shut off transistor in series with the second mirror transistor and the input transistor of the first stage, a gate of the second shut off transistor being driven by an opamp.

24. The regulator of claim **22**, further including a current source between the resistor divider and the supply voltage.

25. The regulator of claim **22**, further including an NMOS transistor between the first shut off transistor and the input transistor.

26. The regulator of claim **1**, wherein a phase margin of the voltage regulator is at least 60 degrees.

27. The regulator of claim **1**, further including a feedback stage with a resistor divider between the third stage and the first stage, wherein a feedback voltage from the resistor divider controls an amplification of the first stage.

28. The regulator of claim 1, wherein a drop-out voltage of the regulator is no more than approximately 14 millivolts.